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AMENDMENTS IN THE CLAIMS:

1. (Previously Presented) A method of transferring data from a sender process to a plurality of receiver processes, wherein at least one of said processes is described in a hardware description language, said hardware description language incorporating simulation means for simulation of the behaviour of hardware and also incorporating a hardware compiler for deriving hardware which behaves according to said simulation, characterised in that the method uses a language construct which, for a given communication, defines a sender process for sending the communication and defines a plurality of receiver processes each for receiving the communication sent by the sender process, thereby effecting synchronised communication between the sender process and the receiver processes.

2. (Original) A method as claimed in claim 1 which involves carrying out a send algorithm under the control of a pre-emptive scheduler.

3. (Original) A method as claimed in claim 2, characterised in that the scheduler ensures that the send algorithm is carried out without descheduling.

4. (Original) A method as claimed in claim 2, characterised in that a check is made that all of the receiver processes are ready to receive data before data is transferred from the sender process to the receiver processes.

5. (Original) A method as claimed in claim 1 which involves carrying out a receive algorithm under the control of a pre-emptive scheduler.

6. (Original) A method as claimed in claim 5, characterised in that the scheduler ensures that the receive algorithm is carried out without descheduling.

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7. (Original) A method as claimed in claim 1, characterised in that at least one of said processes is embodied in hardware.

8. (Original) A method as claimed in claim 1, characterised in that all of said processes are described in said hardware description language.

9. (Original) A synchronous electrical circuit produced by first simulating at least part of the circuit in accordance with the method of claim 1, and then creating the circuit using said hardware compiler.

10. (Original) A synchronous electrical circuit as claimed in claim 9, which is a digital electronic circuit.

11. (Previously Presented) A hardware description language adapted to simulate the behaviour of at least a sender process and a plurality of receiver processes, and comprising a language construct which, for a given communication, defines a sender process for sending the communication and defines a plurality of receiver processes each for receiving the communication sent by the sender process, thereby effecting synchronised communication between the sender process and the receiver processes.

12. (Original) A hardware description language adapted to carry out the method of claim 1.

13. (Original) A computer readable medium carrying a computer program adapted to carry out the method of claim 1.